

Certificate

UK-G83 issue 2


Type Approval and manufacturer/supplier declaration of compliance with the requirements of Engineering Recommendation G83/2.

SSEG Type reference number	Eversol TLC10K		
SSEG Type	Photovoltaic Inverter		
System Supplier name	Jiangsu Zeversolar New Energy CO., LTD.		
Address	No. 198 Xiangyang Road, Suzhou, 215011 China		
Tel	+86 512 6937 0998	Fax	+86 512 6937 0630
E:mail	service.china@zeversolar.com	Web site	www.zeversolar.com

Maximum rated capacity	Connection Option	
	N/A	kW single phase, single, split or three phase system
	10.0	kW three phase (Eversol TLC10K)
	N/A	kW two phases in three phase system
	N/A	kW two phases split phase system

SSEG manufacturer/supplier declaration.

I certify on behalf of the company named above as a manufacturer/supplier of Small Scale Embedded Generators, that all products manufactured/supplied by the company with the above SSEG Type reference number will be manufactured and tested to ensure that they perform as stated in this Type Verification Test Report, prior to shipment to site and that no site modifications are required to ensure that the product meets all the requirements of G83/2.

Signed		On behalf of	Jiangsu Zeversolar New Energy CO., LTD.
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The result of the G83/2 tests are summarized in this certificate.

Zeversolar declares that the units installed in UK market and set for G83/2 operations are characterized by the following features:

- The internal specification and parameters are set to be compliant with: Engineering Recommendation G83 issue 2, August 2012
- These parameters can't be changed by user, an installer or by any person other than Zeversolar (password protected)

POWER QUALITY

Harmonic current emissions as per BS EN 61000-3-2						
SSEG rating per phase (rpp)			3.33	KW	NV=MV*3.68/rpp	
Harmonic	At 45-55% of rated output		100% of rated output			
	Measured Value (MV) in Amps	Normalised Value (NV) in Amps	Measured Value (MV) in Amps	Normalised Value (NV) in Amps	Limit in BS EN 61000-3-2 in Amps	Higher limit for odd harmonics 21 and above
2	0.052	0.058	0.026	0.029	1.080	
3	0.02	0.022	0.022	0.025	2.300	
4	0.011	0.012	0.015	0.017	0.430	
5	0.1	0.112	0.119	0.133	1.140	
6	0.014	0.016	0.009	0.010	0.300	
7	0.049	0.055	0.095	0.106	0.770	
8	0.051	0.057	0.02	0.022	0.230	
9	0.012	0.013	0.012	0.013	0.400	
10	0.048	0.054	0.019	0.021	0.184	
11	0.036	0.040	0.074	0.083	0.330	
12	0.011	0.012	0.009	0.010	0.153	
13	0.031	0.035	0.074	0.083	0.210	
14	0.015	0.017	0.014	0.016	0.131	
15	0.009	0.010	0.01	0.011	0.150	
16	0.011	0.012	0.017	0.019	0.115	
17	0.024	0.027	0.062	0.069	0.132	
18	0.008	0.009	0.01	0.011	0.102	
19	0.029	0.032	0.064	0.072	0.118	
20	0.008	0.009	0.012	0.013	0.092	
21	0.01	0.011	0.009	0.010	0.107	0.160
22	0.01	0.011	0.009	0.010	0.084	
23	0.031	0.035	0.05	0.056	0.098	0.147
24	0.011	0.012	0.009	0.010	0.077	
25	0.034	0.038	0.049	0.055	0.090	0.135
26	0.01	0.011	0.007	0.008	0.071	
27	0.008	0.009	0.01	0.011	0.083	0.124
28	0.009	0.010	0.011	0.012	0.066	
29	0.021	0.024	0.03	0.034	0.078	0.117
30	0.008	0.009	0.009	0.010	0.061	
31	0.024	0.027	0.023	0.026	0.073	0.109
32	0.01	0.011	0.008	0.009	0.058	
33	0.01	0.011	0.01	0.011	0.068	0.102
34	0.011	0.012	0.011	0.012	0.054	
35	0.028	0.031	0.008	0.009	0.064	0.096
36	0.009	0.010	0.009	0.010	0.051	
37	0.033	0.037	0.013	0.015	0.061	0.091
38	0.009	0.010	0.01	0.011	0.048	
39	0.012	0.013	0.008	0.009	0.058	0.087
40	0.008	0.009	0.011	0.012	0.046	

Note the higher limits for odd harmonics 21 and above are only allowable under certain conditions, if these higher limits are utilised please state the exemption used as detailed in part 6.2.3.4 of BS EN 61000-3-2 in the box below.

Voltage Fluctuations and Flicker as per BS EN 61000-3-3

	Starting			Stopping			Running	
	dmax	dc	d(t)	dmax	dc	d(t)	Pst	Plt 2 hours
Measured Values	1.03%	0.51%	1.10%	0.81%	0.84%	0.82%	0.248	0.222
Normalised to standard impedance and 3.68kW for multiple units	1.14 %	0.57 %	1.22 %	0.90 %	0.93%	0.91 %	0.278	0.249
Limits set under BS EN 61000-3-2	4%	3.3%	3.3% 500ms	4%	3.3%	3.3% 500ms	1.0	0.65
Test start date	2014.06.03			Test end date			2014.06.03	
Test location	Audix Technology (Wujiang) Co., Ltd.							

Test level	DC injection			Power factor *		
	10%	55%	100%	216.2 V	230 V	253 V
Measured value	28.2mA	32.5mA	31.3mA	0.995	0.997	0.998
as % of rated AC current	0.19%	0.22%	0.22%	-	-	-
Limit	0.25%	0.25%	0.25%	>0.95	>0.95	>0.95

* Measured at three voltage levels and at full output. The voltage to be maintained within $\pm 1.5\%$ of the stated level during the test.

PROTECTION

Frequency tests

Function	Setting		Trip test		"No trip tests"	
	Frequency	Time delay	Frequency	Time delay	Frequency/time	Confirm no trip
U/F Stage 1	47.5Hz	20s	47.50Hz	20.15s	47.7Hz/25s	No trip
U/F Stage 2	47.0Hz	0.5s	47.01Hz	0.62s	47.2Hz/19.98s	No trip
					46.8Hz/0.48s	No trip
O/F Stage 1	51.5 Hz	90s	51.51Hz	90.20s	51.3Hz/95s	No trip
O/F Stage 2	52.0 Hz	0.5s	52.01Hz	0.62s	51.8Hz/89.98s	No trip
					52.2Hz/0.48s	No trip

Voltage tests

Function	Setting		Trip test		"No trip tests"	
	Voltage	Time delay	Voltage	Time delay	Voltage/time	Confirm no trip

U/V Stage 1 L1	200.1V	2.5s	199.8V	2.61s	204.1V/3.5s	No trip
U/V Stage 1 L2	200.1V	2.5s	198.9V	2.61s	204.1V/3.5s	No trip
U/V Stage 1 L3	200.1V	2.5s	201.0V	2.62s	204.1V/3.5s	No trip
U/V Stage 2 L1	184.0V	0.5s	183.4V	0.62s	188V/2.48s	No trip
U/V Stage 2 L2	184.0V	0.5s	184.8V	0.62s	188V/2.48s	No trip
U/V Stage 2 L3	184.0V	0.5s	184.2V	0.62s	188V/2.48s	No trip
					180V/0.48s	No trip
O/V Stage 1 L1	262.2V	1.0s	264.1V	1.10s	258.2V/2.0s	No trip
O/V Stage 1 L2	262.2V	1.0s	262.4V	1.11s	258.2V/2.0s	No trip
O/V Stage 1 L3	262.2V	1.0s	262.9V	1.11s	258.2V/2.0s	No trip
O/V Stage 2 L1	273.7V	0.5s	275.2V	0.62s	269.7V/0.98s	No trip
O/V Stage 2 L2	273.7V	0.5s	274.6V	0.61s	269.7V/0.98s	No trip
O/V Stage 2 L3	273.7V	0.5s	275.8V	0.62s	269.7V/0.98s	No trip
					277.7V/0.48s	No trip

Note for Voltage tests the Voltage required to trip is the setting $\pm 3.45V$. The time delay can be measured at a larger deviation than the minimum required to operate the protection. The No trip tests need to be carried out at the setting $\pm 4V$ and for the relevant times as shown in the table above to ensure that the protection will not trip in error.

Loss of Mains test

Note as an alternative, inverters can be tested to BS EN 62116. The following sub set of tests should be recorded in the following table.

Balancing load on islanded network	33% -5% Q Test 22	66% -5% Q Test 12	100% -5% P Test 5	33% +5% Q Test 31	66% +5% Q Test 21	100% +5% P Test 10
Trip time. Limit is 0.5 seconds	0.38s	0.44s	0.37s	0.40s	0.35s	0.28s

Frequency change, Stability test

	Start Frequency	Change	End Frequency	Confirm no trip
Positive Vector Shift	49.5Hz	+9 degrees		No trip
Negative Vector Shift	50.5Hz	-9 degrees		No trip

Positive Frequency drift	49.5Hz	+0.19Hz/sec	51.5Hz	No trip
Negative Frequency drift	50.5Hz	-0.19Hz/sec	47.5Hz	No trip

Re-connection timer

Test should prove that the reconnection sequence starts after a minimum delay of 20 seconds for restoration of voltage and frequency to within the stage 1 settings of table 1.

Time delay setting	Measured delay	Checks on no reconnection when voltage or frequency is brought to just outside stage 1 limits of table 1.			
30s	30s	At 266.2V	At 196.1V	At 47.4Hz	At 51.6Hz
Confirmation that the SSEG does not reconnect.		No reconnect	No reconnect	No reconnect	No reconnect

FAULT LEVEL CONTRIBUTION

For a directly coupled SSEG			For a Inverter SSEG		
Parameter	Symbol	Value	Time after fault	Volts	Amps
Peak Short Circuit current	i_p	-	20ms	186V	14.67A
Initial Value of aperiodic current	A	-	100ms	74V	6.81A
Initial symmetrical short-circuit current*	I_k	-	250ms	56V	5.16A
Decaying (aperiodic) component of short circuit current*	i_{bc}	-	500ms	31V	2.90A
Reactance/Resistance Ratio of source*	X/R	-	Time to trip	0.05	In seconds

SELF-MONITORING SOLID STATE SWITCHING

Not applicable as electro-mechanical relays are used.